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Abstract
Nowadays, high performance in circuit design is highly emphasized and thus structural regularity and circuit delay predictability of Programmable Logic Array (PLA) have become well suited for automation designs of logic gates. Dynamic programmable logic array (DPLA), on the other hand, has the benefits of high speed performance and low power consumption while maintaining the original advantages of PLA. Many new DPLA structures have been widely adopted for implementing control logic gates in high-end processors.
Unfortunately, a single DPLA structure cannot be applied to all circuits. Therefore, how should an appropriate circuit structure be chosen when implementing a circuit with DPLA? How to properly adjust the input/output buffer, inter buffer and clock buffer based on the circuit size and input function? To address these questions, our system is capable of creating a layout and automatically generating a netlist file to facilitate the subsequent verification work (e.g. LVS, PEX, etc), based on the DPLA structure chosen with the design constrain specificed by the user and the cell library that we designed earlier. The silicon compiler that we completed has the following characteristics:
1. Capable of evaluating the loading based on the PLA input function：
Our system can perform an analysis on the circuit and evaluate the loading capacitance/resistance value based on the PLA input function. Then, it can choose an appropriate leaf cell from the DPLA cell library based on the evaluated loading value.

2. Generating a DPLA layout and a netlist file simultaneously：
In order to achieve automation and optimization in the entire DPLA design flow from layout generation to LVS verification, the DPLA compiler designed by our system can automatically generate a corresponding netlist file, in addition to a DPLA layout.

3.Containing various DPLA circuit structures：
Our system has many different DPLA circuit structures to fulfill the requirements of extensive circuit application and operating frequency.

4.Flexible cell library：
Each basic element (i.e. ,input/output buffer, inter buffer, clock buffer, and AND/OR plane transistor) in the cell library that our system has created for different structures contains various leaf cells with different transistor sizes. Moreover, since global routing is already considered in each leaf cell, global routing doesn't need to be performed again after compiling.

5.DFM (design for manufacturability)：
In addition to adding the required dummy pattern in each leaf cell, our system automatically adds dummy pattern at each layer to fulfill the requirement of DRC and to improve manufacturability.
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